

Appl. No. 10/065,220
Amdt dated November 08, 2004
Amendment After Notice of Allowance dated August 06, 2004

Amendments to the Claims

This listing of claims will replace all prior versions and listing of claims in the application:

Listing of Claims:

1. (cancelled)
2. (previously presented) An integrated circuit comprising:
a memory array having a plurality of memory banks;
a plurality of comparator units, each associated with one memory bank; and
a BIST control unit coupled to the memory array, the BIST control unit generates control signals and a test pattern for testing the memory array, wherein the comparator units facilitate testing the memory banks simultaneously by having each comparator unit comparing a word read from its associated memory bank with the test pattern written.
3. (previously presented) The integrated circuit of claim 2 wherein the memory banks occupy a common address space and the BIST control unit generates addresses in the common address space.
4. (cancelled)
5. (cancelled)

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6. (previously presented) The integrated circuit of claim 2 wherein the memory banks can have different sizes.
7. (previously presented) The integrated circuit of claim 2 wherein the comparator units store faulty addresses.
8. (cancelled)
9. (currently amended) The integrated circuit of claim 2, 3, 6 or 7 wherein the BIST control unit receives test results from the comparator units.
10. (original) The integrated circuit of claim 9 wherein the BIST control unit outputs the test results serially in response to an input clock signal.
11. (original) The integrated circuit of claim 10 wherein the test results comprise addresses of faulty words.
12. (previously presented) The integrated circuit of claim 10 wherein the test results comprise addresses of faulty words and locations of faulty bits within the faulty words.
13. (previously presented) The integrated circuit of claim 9 wherein the test results comprise addresses of faulty words.

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14. (previously presented) The integrated circuit of claim 9 wherein the test results comprise addresses of faulty words and locations of faulty bits within the faulty words.

15. (previously presented) An integrated circuit comprising:
a memory array having a plurality of memory banks, wherein a memory bank includes a plurality of memory cells having first and second ports;
a plurality of comparator units, each associated with one memory bank; and
a BIST control unit coupled to the memory array, the BIST control unit generates control signals and a test pattern for testing the memory array, wherein the comparator units facilitate testing the memory banks simultaneously by having each comparator unit comparing a word read from its associated memory bank with the test pattern written.

16. (previously presented) The integrated circuit of claim 15 wherein a test mode for testing can be either single port or dual port test mode.

17. (previously presented) An integrated circuit comprising:
a memory array having a plurality of memory banks;
a plurality of comparator units, a comparator unit being coupled to a memory bank for comparing a test pattern written to the memory bank against data read from the memory bank, wherein the comparator unit comprises a test control unit and a testing circuit, the test control unit is coupled to an access control circuit and a refresh control unit; and

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a BIST control unit coupled to the plurality of comparator units for testing the plurality of memory banks in parallel, the BIST control unit provides test control signals and the test pattern to the comparator units.

18. (previously presented) The integrated circuit of claim 17 wherein the memory banks include a plurality of memory cells having first and second ports and wherein a test mode for testing can be either single port or dual port test mode.

19. (currently amended) The integrated circuit of claim 17 or 18 wherein the test control signals comprise addresses of memory words to be tested.

20. (previously presented) The integrated circuit of claim 19 wherein the memory banks can have different sizes.

21. (previously presented) The integrated circuit of claim 19 wherein the comparator units store faulty addresses.

22. (previously presented) The integrated circuit of claim 20 wherein the BIST control unit receives test results from the comparator units.

23. (previously presented) The integrated circuit of claim 22 wherein the comparator units store faulty addresses.

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24. (cancelled)

25. (previously presented) An integrated circuit comprising:
a memory array which includes a plurality of memory banks;
a plurality of comparator units, wherein at least one comparator is associated with one memory bank; and
a BIST control unit coupled to the memory array, the BIST control unit receives input control signals and, in response to the input control signals, causes the integrated circuit to be in test mode and generates test control signals and a test pattern, wherein each comparator unit compares a word read from its associated memory bank with the test pattern written.

26. (previously presented) The integrated circuit of claim 25 wherein memory cells of the memory array comprise dual-port memory cells and the test mode can be either single port or dual port test mode.

27. (previously presented) The integrated circuit of claim 25 wherein some or all the plurality of memory banks can be of different sizes.

28. (previously presented) The integrated circuit of claim 27 wherein memory cells of the memory array comprise dual-port memory cells and the test mode can be either single port or dual port test mode.

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29. (currently amended) The integrated circuit of claim 25, 26, 27 or 28 wherein the test control signals comprise memory addresses to be tested.

30. (previously presented) The integrated circuit of claim 29 wherein the test mode generates test patterns selected from march, checkerboard, wordline strip, blanket, or a combination thereof.

31. (previously presented) The integrated circuit of claim 29 wherein defective addresses are stored in the comparator units.

32. (previously presented) The integrated circuit of claim 29 wherein the BIST control unit outputs the test results comprising addresses of faulty words.

33. (previously presented) The integrated circuit of claim 29 wherein the BIST control unit outputs the test results comprising addresses of faulty words and locations of faulty bits within the faulty words.

34. (previously presented) The integrated circuit of claim 3 wherein the comparator units store faulty addresses.

35. (previously presented) The integrated circuit of claim 6 wherein the comparator units store faulty addresses.